Updates to IEEE 1547-2003 DER Modeling Assumptions

Planning Advisory Committee

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Purpose

- Discuss the new DER modeling assumptions for legacy DERs (installed under IEEE Standard 1547-2003)
  - Why are we revising the parameters?
  - What was the approach used for developing the DER modeling assumptions?
  - What are the new voltage trip settings?
  - How do these updated DER trip settings impact simulation results?

BACKGROUND

Background

- In the TPCET Pilot study, ISO-NE conservatively assumed that DERs interconnected under IEEE 1547-2003 would trip after 6 cycles of a voltage under 0.88 per unit
- These assumptions showed widespread DER tripping throughout New England for design contingencies
- The worst fault was a single-line-to-ground (SLG) fault with breaker failure on the SEMA/RI 345 kV system, which resulted in 1,855 MW of DER tripping in the Spring Weekend Mid-Day Minimum Load study condition
- Majority of the DERs that tripped for that fault were IEEE 1547-2003 DERs
- In May 2022, ISO-NE began discussions with PAC on re-assessing protection assumptions for IEEE 1547-2003 DERs

IEEE 1547-2003 Protection Assumptions

- Transmission Planning has looked into the original inverter settings for the IEEE 1547-2003 DER
- At right is a sample set of trip settings from a common inverter manufacturer, for inverters installed under the IEEE 1547-2003 standard
- This manufacturer sets the voltage for the fastest trip timer to 50% and not 88%, supporting the idea that DER trips at a lower voltage than what was assumed in the TPCET Pilot Study

Voltage (V)	Voltage (%)	Trip Timer (sec)
>288	>120%	0.12
>264	>110%	1
<211	<88%	2
<120	<50%	0.12

IEEE 1547-2003 Protection Assumptions

- Evidence from inverter manufacturers and other sources indicates that some DER installations do trip for transmission faults as short as 6 cycles
- However, many inverters will ride through voltages down to 50% for short periods of time
  - The 88% voltage assumption used in the TPCET Pilot Study appears to have been too conservative
- The assumption used in simulations may need to be higher than 50% to approximate tripping for single-phase faults
- ISO-NE will be revising these assumptions, and expects that the revised assumptions will show smaller amounts of DER tripping than what was observed in the TPCET Pilot Study

MODELING CHALLENGES

Modeling Challenges

- PSS®E is a fundamental frequency, positive sequence dynamic simulation software
- PSSE assumes a balanced system at all times and the positive sequence values are an approximation of three-phase behavior. An approximate equivalent fault impedance is used to simulate unbalanced faults like a single-line-to-ground fault
- Voltage in stability simulations doesn't necessarily correspond to voltage seen at the terminals of a single-phase inverter (like most residential inverters)
- Results will be an approximation, at best – due to several factors, such as sub-cycle phenomena, varying protection settings among inverter manufacturers, three-phase vs. single-phase behavior, and voltage variations along a distribution feeder

Modeling Challenges

- Since most residential rooftop DERs are connected by single phase inverters, only the DERs connected to the phases affected by the fault may trip
- For example, for faults affecting a single phase, only the DERs on the phase affected by the fault (roughly 1/3 of the total amount of single-phase DERs) may trip. DERs connected to the healthy phases may remain online
- The table on the next slide shows examples of some faults, voltages on individual phases, the corresponding positive sequence voltage in PSS®E simulation, and the proportion of DERs expected to trip

Modeling Challenges

This table is only an example to illustrate that some DERs may trip and others may not, depending on the voltages at different phases, in response to a system disturbance

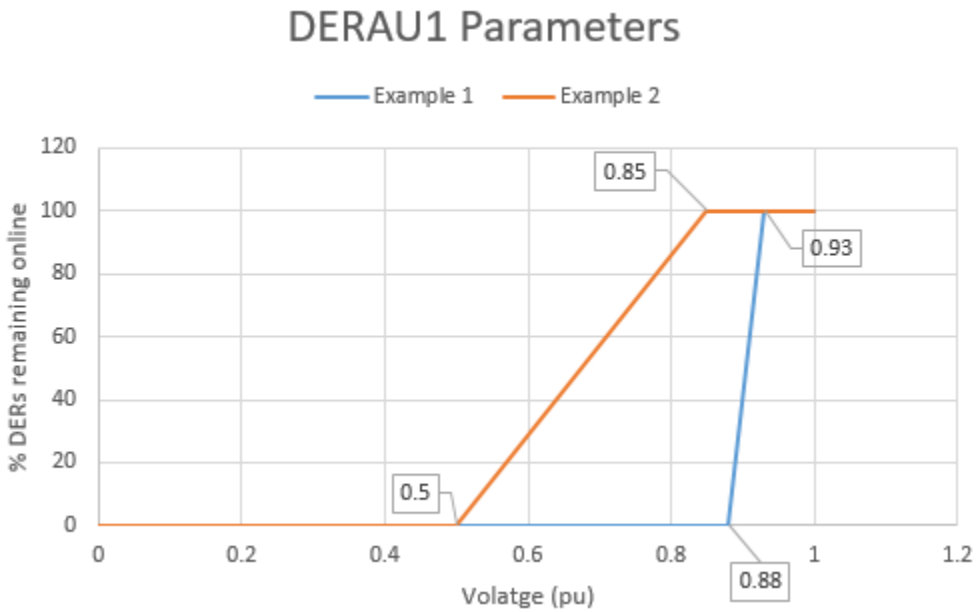
Balanced/ Unbalanced Condition	System Condition	Voltage on individual phases (p.u.)	Positive Sequence Voltage in PSS®E (p.u.)	DERs expected to trip
Balanced	Steady State (Pre-Disturbance condition)	Va ~ 1.0, Vb ~ 1.0, Vc ~ 1.0	V ~ 1.0	
Unbalanced	Bolted Single Line-To-Ground fault on Phase A	Va ~ 0, Vb ~ 1.0, Vc ~ 1.0	V ~ 0.67	• 1/3rd of Single Phase Inverters would trip (Only those connected to Phase A) • All three Phase Inverters would trip
Unbalanced	Single Line-To-Ground fault on Phase A with fault impedance	Va ~ 0.5, Vb ~ 1.0, Vc ~ 1.0	V ~ 0.83	• 1/3rd of Single Phase Inverters would trip (Only those connected to Phase A) • All three Phase Inverters would trip
Unbalanced	Single Line-To-Ground fault on Phase A with fault impedance	Va ~ 0.6, Vb ~ 1.0, Vc ~ 1.0	V ~ 0.87	• All DERs would remain online
Unbalanced	Double Line-To-Ground fault with fault impedance	Va ~ 0.5, Vb ~ 0.5, Vc ~ 1.0	V ~ 0.67	• 2/3rd of Single Phase Inverters would trip (Only those connected to Phase A or Phase B) • All three Phase Inverters would trip
Balanced	Bolted Three phase fault	Va ~ 0, Vb ~ 0, Vc ~ 0	V ~ 0	• All DERs would trip
Balanced	Three phase fault with fault impedance	Va ~ 0.5, Vb ~ 0.5, Vc ~ 0.5	V ~ 0.5	• All DERs would trip

Modeling Challenges

- The response of devices connected to a single phase cannot be captured well in a positive sequence software under all scenarios
  - Under balanced conditions, the voltages in the PSS®E simulation match the voltages at individual phases
  - However, under unbalanced conditions, the positive sequence voltage in PSS®E does not represent the voltages at the individual phases
- The bookends are highlighted with green boxes on the previous slide
  - If the positive sequence voltage is above 0.83 per unit, all the DERs connected to that bus would remain online
  - If the positive sequence voltage is below 0.5 per unit, all DERs connected to that bus would trip
  - For positive sequence voltages between 0.5 to 0.83 per unit, for more than 6 cycles, some DERs would trip and some would remain online
- There is no way to exactly model DER tripping in PSS®E
  - Reasoning: Positive sequence voltage could be the same for different types of faults. For example, in both rows 2 and 5, the positive sequence voltage is 0.67 p.u., but either 1/3 or 2/3 of DERs would trip depending on the type of fault
  - In addition to this, DERs have been known to trip due to various other reasons like phase-locked loop (PLL) loss of synchronism, sub-cycle transient ac overvoltage and frequency-related phenomena
- With these challenges in mind, the next hurdle is the limitations within the DER model in PSS®E

Modeling Challenges

- The model used for DER in PSS®E has only limited parameters available to model the partial tripping behavior as discussed in the previous slide, where some DERs would trip and some would remain online
- A high and low voltage assumption can be specified, but the model can only linearly interpolate between these two points, as shown in the figure below



DEVELOPMENT OF IEEE 1547-2003 DER TRIP ASSUMPTIONS

Development of IEEE 1547-2003 DER Trip Assumptions: Outline

1 Sense data	Sense data showed clusters of rooftop solar dropping out for ~5-6 minutes in the SEMA region
2 PMU/PI data	PMU data corroborated Sense data. Disturbance was observed at the transmission level as well
3 Fault	The event was traced back to a fault on a 115 kV transmission line
4 Simulation	Similar conditions were simulated in PSS®E and tested with different DER trip assumptions
5 DER Model	DER trip assumptions used in the TPCET pilot study and the revised assumptions were compared with real time

Development of IEEE 1547-2003 DER Trip Assumptions: Sense Data

1 Sense data

Sense data showed clusters of rooftop solar inverter dropping out for ~5-6 minutes in the SEMA region

- A company named ‘Sense’ uses machine learning to identify unique signatures of electronic devices. They were able to provide data, anonymized by ZIP code, showing rooftop solar inverters tripping
- Sense data showed clusters of rooftop solar inverters dropping off at the same time for about 5 to 6 minutes on 7/27/2021 at 3:27 PM

Figure: Solar dropouts in kW on 7/27/2021 at 03:27 PM for a fault at X

Note that Sense data is not available on every rooftop solar installation. However, this gives an indication that a considerable number of inverters tripped

Development of IEEE 1547-2003 DER Trip Assumptions: PMU/PI Data

2 PMU/PI data

PMU data corroborated Sense data. Disturbance was observed at the transmission level as well

- At the same time, disturbance was observed at the transmission level as well. The figure below shows the voltage drop observed at a PMU, located on a nearby 345 kV bus

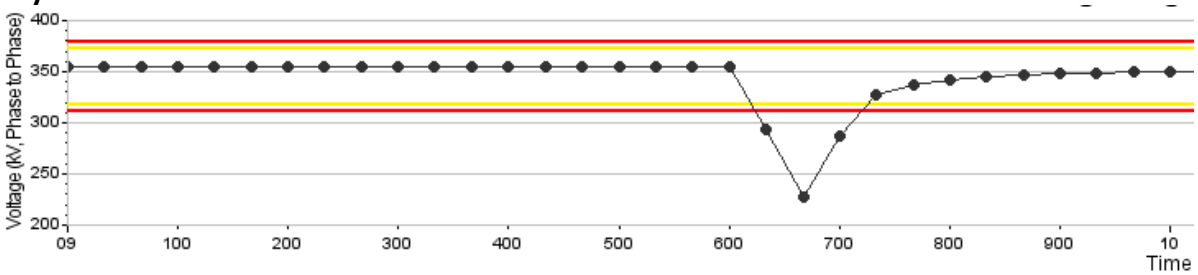


Figure shows the positive sequence line-line voltage (kV) over a time period of 1 second

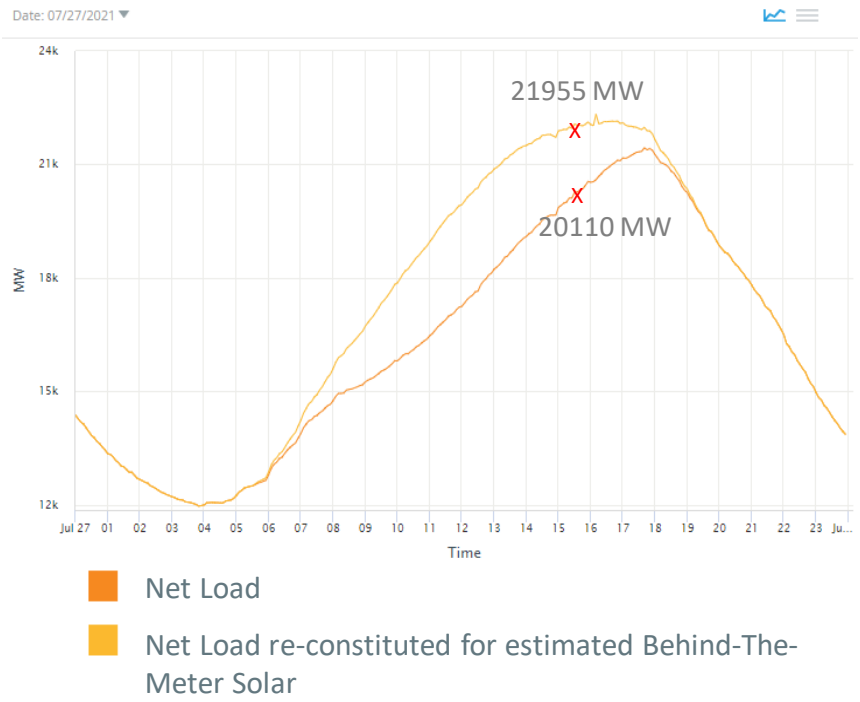
- Further, PI data showed a 50 MW increase in load above the trend of pre-fault load, for up to 4-5 minutes after the fault
- Shortly after that, load had returned to the expected trend
- This matches the typical behavior of IEEE 1547-2003 DERs, which are set to remain offline for about 5 minutes after the fault and then come back online

Development of IEEE 1547-2003 DER Trip Assumptions: Fault

3 Fault

The event was traced back to a fault on a 115 kV transmission line in SEMA

- The fault occurred on a 115 kV transmission line in SEMA at 03:27 PM EST
- The fault occurred on a hot day (highest temperature was around 89° F).
- Based on solar irradiance, solar output was approximately 70% of nameplate ratings
- The conditions were similar to the Summer Mid-Day Peak (High Renewables) Scenario used in the TPCET Pilot Study



Development of IEEE 1547-2003 DER Trip Assumptions: Simulation

4 Simulation

Similar conditions were simulated in PSS®E and tested with different DER trip assumptions

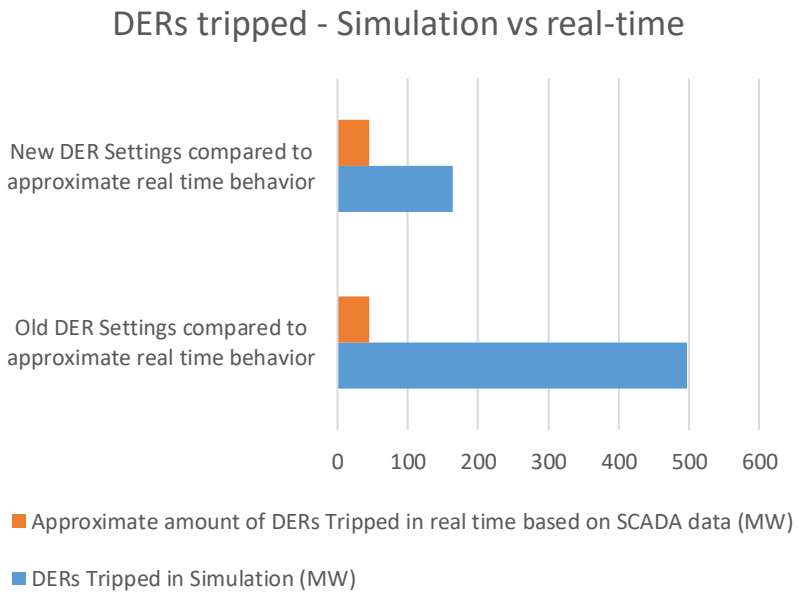
- Although we do not have exact trip information from individual distribution connected rooftop solar inverters, with the indirect information available from all these sources, we compared our simulation results with the approximate DER tripping observed in real-time
- The TPCET Summer Mid-Day Peak (High Renewables) Scenario case was adjusted to match the dispatch conditions in the local area around the fault
- The same 115 kV transmission line fault was tested on this case, with both old and revised IEEE 1547-2003 DER trip settings

Development of IEEE 1547-2003 DER Trip Assumptions: DER Model

5 DER Model

DER trip assumptions used in the TPCET pilot study and the revised assumptions were compared with real time behavior

- The proposed DER settings match well with the approximate real time DER tripping behavior
- Although we may be still overestimating the DER tripping a little bit, DERs have been known to trip due to various other reasons like phase-locked loop (PLL) loss of synchronism, sub-cycle transient ac overvoltage and frequency-related phenomena that cannot be modeled in PSS®E
- In addition to that, given the modeling challenges discussed earlier, this is as close as we can get



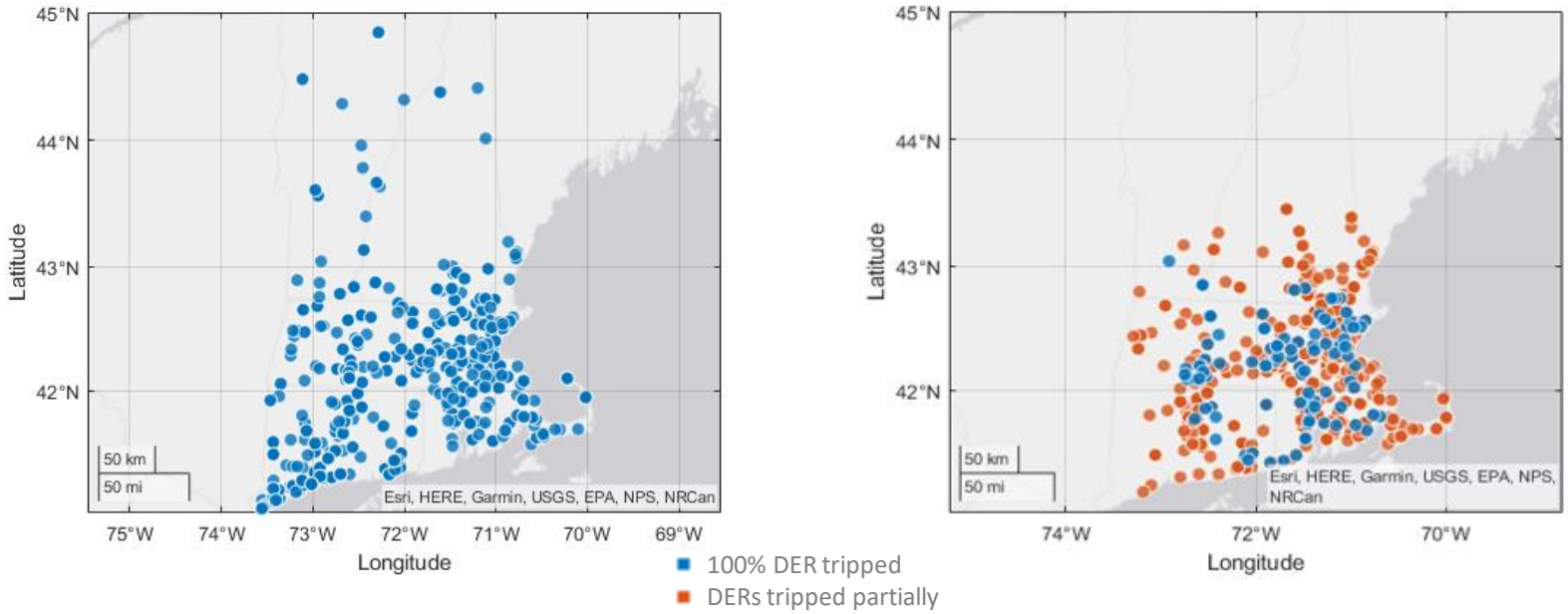
IMPACT OF REVISED IEEE 1547-2003 DER TRIP ASSUMPTIONS

Impact Of Revised IEEE 1547-2003 DER Trip Assumptions

- ISO-NE revisited the fault that caused considerable DER tripping in the TPCET Pilot study – a single-line-to-ground (SLG) fault with breaker failure on the SEMA/RI 345 kV in the Spring Weekend Mid-Day Minimum Load study conditions

Simulation results with old assumptions: 1,855 MW of DERs tripped, out of which 1,495 MW were IEEE 1547-2003 <1 MW DERs

Simulation results with new Assumptions: 950 MW of DERs tripped, out of which 570 MW were IEEE 1547-2003 <1 MW DERs



NEXT STEPS

Next Steps

- Update the Transmission Planning Technical Guide (TPTG) to reflect the revision to DER modeling assumptions
- Implement the revised DER trip assumptions in future Transmission Planning studies - Needs Assessments, Solutions Studies and competitive transmission requests for proposals (RFPs)

Questions

APPENDIX

Appendix: Revised IEEE 1547-2003 DER Trip Assumptions

- Revised voltage trip logic parameters for 1547-2003 DER inverters are listed below
- P5: R-DER having legacy inverters reflective of IEEE Std. 1547-2003

DERAU1 Model Parameter	IEEE 1547-2003 (Used in TPCET Pilot Study)	Revised IEEE 1547-2003 Trip Settings
vl0	0.88	0.5
vl1	0.93	0.85
tvl0	0.1	0.1
tvl1	0.1	0.1

- P7: U-DER having legacy inverters reflective of IEEE Std. 1547-2003

DERAU1 Model Parameter	IEEE 1547-2003 (Used in TPCET Pilot Study)	Revised IEEE 1547-2003 Trip Settings
vl0	0.88	0.83
vl1	0.93	0.88
tvl0	0.1	0.1
tvl1	0.1	0.1

- For detailed modeling information of the DERAU1 model, refer to the TPCET CEII Supplement document posted here - https://smd.iso-ne.com/operations-services/ceii/pac/2021/08/tpcet_ceii_document.pdf